Remarks

Re: Specification (1/2)

The Specification has been supplemented as required by 1/2.
The section "Background Art" has been upgraded with additional explanations of major differences between the present invention versus the closest background art anticipated by Bogdan (U.S. Patent No. 6, 148, 052). These additional explanations facilitate easier examination of the present invention claims.

RE: Claim Objections (3/4)

In response to the Claim Objections 3/4, related equivalents of claims 2/17 have been corrected.

RE: Claim Rejections (5)

In order to facilitate more convenient examination process, the applicant has rewritten claim 1 by including claim 2 limitation into the amended claim 1 and canceled the claim 2 entirely. Since the previously presented claim 2 has been generally accepted, the currently amended claim 1 shall be acceptable as well.
Consequently having acceptable base claim 1, shall enable cancellation of all the rejections of the intervening claims 3-41.

While cooperating in making the process easier; the applicant explains below that all the rejection arguments are based on the explained below misconceptions and even the original claims could be successfully defended.

The detailed action writes:

"Claims 1, 4-10 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Bogdan (U.S. Patent No. 6, 148, 052).

Referring to claim 1, Bogdan discloses a digital phase detector (DPD circuit, abstract, line 1), wherein the digital phase detector comprises:

a frame measurement configuration (ring counter 15 in Figure 2) for counting the first signal clock (signal output from 50 in Figure 2) during every frame of a second signal (VCXO-RCRST signal in Figure 2), and for buffering (by using ring counter buffer 16 in Figure 2) the counted value until it is read by a phase processing unit (CU 8 in Figure 1)."

The above citation contains the listed below major misconceptions:

1. The "signal output from 50 in Figure 2" is the output of the auxiliary internal free running ring oscillator and is fundamentally different than the "first signal clock" which is coming from outside of the DPD circuit and is defined entirely by an external circuit.
2. Since the "signal output from 50 in Figure 2" is proven to be fundamentally different than the "first signal clock", "the ring counter 15 in Figure 2" performs fundamentally different functions and can never be considered "a frame measurement configuration".
3. The "VCXO-RCRST signal in Figure 2" is the internal reset signal generated by the phase processing unit (CU 8) and its only purpose is to make sure that the Ring Counter never overflows during the measurement periods $t_0 - t_1$, $t_0 - t_2$, $t_0 - t_3$ shown in the FIG.7 .

Consequently such DPD internal reset signal does not bear any resemblance and has nothing in common with the "frame of a second signal" which is defined entirely by the externally generated second signal.

Due to the misconceptions explained above, the entire above citation and the rejection of the previous claim 1 are incorrect as well.

The detailed action further writes:

"Referring to claim 4, Bogdan discloses a phase capture register (ROC 5 or 7 in Figure 1) for capturing a state of outputs of serially connected gates (50 in Figure 2) which the first signal clock (output from 50 in Figure 2) is propagated through, at the leading edge of the second signal (VCXO-RCRST signal in Figure 2) frame."

Similarly as it has been proven above:

Since the first signal clock is never propagated through the "serially connected gates (50 in Figure 2)" and the "(VCXO-RCRST signal in Figure 2)" has nothing in common with the second signal frame, the previously presented claim 4 represents subject matter fundamentally different than the U.S. Patent No. 6, 148, 052.

Still next citation "Referring to claim 5, Bogdan discloses a phase capture register (ROC 5 or 7 in Figure 1) for capturing a rise of the second signal frame (VCX-RCRST signal in Figure 2) by multiple outputs of serially connected gates which the first signal clock (output from 50 in Figure 2) is propagated through.",

repeats the above misconceptions concerning the first signal clock and the second signal frame and supplements them with other fundamental misconception explained below. The U.S. Patent No. 6, 148, 052 is always limited to capturing multiple outputs of serially connected gates ER (output from 50 in Figure 2) by another signal, but never does any reverse capturing of another signal "by multiple outputs of serially connected gates" coming from the "(output from 50 in Figure 2)".

Still next citation "Referring to claim 6, Bogdan discloses a phase capture register (ROC 5 or 7 in Figure 1) for capturing a state of outputs of serially connected gates which the second signal clock is propagated through, by the leading edge of the first signal frame", is based on the explained below fundamental misconceptions:

1. Since the serially connected gates are free running, they can never propagate any second signal clock.
2. Since the second signal is generally represented by its frame only, alleged second signal clock is usually unavailable.

Still next citation "Referring to claim 7, Bogdan discloses a phase capture register (ROC 5 or 7 in Figure 1) for capturing a rise of the first signal clock, by multiple outputs of serially connected gates which the second signal clock is propagated through.", repeats the above misconceptions related to "the second signal clock" and supplements them with other misconception explained below.

The U.S. Patent No. 6, 148, 052 is always limited to capturing multiple outputs of serially connected gates ER (output from 50 in Figure 2) by another signal, but never involves any

reverse capturing of another signal "by multiple outputs of serially connected gates" coming from the "(output from 50 in Figure 2)".

Still other citation states "Referring to claims 8-10, Bogdan discloses a digital phase detector wherein the digital phase detector comprises and open ended line / a ring oscillator / a delay locked loop of serially connected gates (50 in Figure2)".
Since the rejections of the previously presented claims 4-7 have been based on the major misunderstanding of the "serially connected gates (50 in Figure2)", these rejections are incorrect and cannot justify any rejection of the dependent claims 8-10.

Still next citation " Referring to claim 17, Bogdan discloses that said first clock counting is enabled (enabling the VCXO_RCRST signal in Figures 1 and 2) by opening a logical gate (using CU8 in Figure 1) which controls an application of the first clock (output of 50 in Figure 2) to counter's (ring counter 15 in Figure 2) clocking input; and disabled (disabling the VCXO_RCRST signal) by closing a logical gate which controls an application of the first clock to counters clocking input.", repeats the above incorrect allegation that the first signal clock can be provided by the "(output of 50 in Figure 2)" and supplements it with other misconception explained below:

The VCXO_RCRST signal (previously alleged to be the second signal frame) is now alleged to be an enabling/disabling signal for the ROC clocking input driven by the "(output of 50 in Figure 2)", while in reality there is no any enabling/disabling gate or signal on the ROC clocking input and the VCXO_RCRST simply is the ROC reset signal applied simultaneously to all the ROC Flip-Flops.
Therefore the above citation cannot justify the rejection of the claim 17.

Re: Allowable Subject Matter (6)

The applicant has rewritten claim 1 by including claim 2 limitation into the amended claim 1 and canceled the claim 2 entirely.
Since the previously presented claim 2 has been generally accepted, the currently amended claim 1 shall be acceptable as well.
Consequently having acceptable base claim 1, shall enable cancellation of all the rejections and objections concerning the intervening claims 3-41.

Re: Conclusion

Based on the above clarifications, it is thus respectfully submitted that the invention taught and defined herein by the claims embodies patentable subject matter. The Examiner is earnestly solicited to give favourable reconsideration to this application and pass it to allowance.

Respectfully submitted,

By: J Bogdan, 16Apr04
John W. Bogdan

Specification Amendments

Please replace the corresponding original part of the specification with the amended part provided below.

High Resolution Phase Frequency Detectors

BACKGROUND OF THE INVENTION

1. Field of the invention

This invention is directed to providing high resolution low cost digital phase detectors which can be used in digital phase locked loops (DPLLs) and shall also make possible other replacements of analog circuits by their digital implementations.
The high resolution phase detectors (HRPD) can be used for a wide range of data rates, and for wireless, optical , or wireline transmission and communication systems.

2. Background art

Most of currently used digital phase detectors have resolution limited by a clock cycle time. While some most advanced digital phase detectors allow higher resolutions which are comparable with propagation delays of clock propagating gates, they have other limitations such as: complex algorithms which are conditioned by propagation delays of detector timing circuits, and dependency of their phase resolution on technological process and power supply variations.

The closest background solution is presented by Bogdan (U.S. Patent No. 6,148,052). However this background solution requires additional oscillator circuit implemented with free running ring oscillator having unknown oscillation frequencies dependent on IC process deviations and power supply variations causing propagation delays deviations ranging from -50% to +50%.

Outputs of such additional unpredictable oscillator circuit are used to capture a phase of a first signal frame and a phase of a second signal frame, which need to be subtracted from each other to calculate a phase skew between the first signal frame and the second signal frame. Therefore in addition to the oscillator circuit , said background solution requires:

separate circuits for capturing first signal phase with oscillator outputs while other circuits are used for capturing second signal phase with the oscillator outputs;

additional circuits for subtracting such separately captured first signal phase from second signal phase;

oscillator calibration circuits for counting and capturing oscillator outputs over a predetermined fixed time period;

control unit circuits and subroutines for processing and using the above calibration results for recalculating the above mentioned inter-signal phase skews.

There is a need for digital phase detectors which have simpler algorithms and greater independence versus the propagation delays of the detector timing circuits and the clock propagating gates.

Such much simpler digital phase detectors are provided by the present invention which eliminates the additional free running oscillator and the above mentioned additional circuits and calibration related subroutines. These improvements are achieved by changing principle of operation, as the present invention:

Propagates the first signal clock through serially connected gates and uses outputs of these gates for sensing phase of the second signal or propagates the second signal through serially connected gates and uses outputs of these gates for sensing phase of the first signal clock, instead of using outputs of the additional free running oscillator for capturing phases of the first signal and the second signal.

Since the first signal and the second signal are much more stable than the free running oscillator; the above calibration circuits are replaced by much simpler self-calibration means or by stabilizing propagation delays of the serially connected gates with phase locked loops or

with delay locked loops.

BRIEF SUMMARY OF THE INVENTION

~~1. Purpose of the invention~~

It is an object of present invention to provide digital high resolution phase detectors which are simple and reliable and can be used in variety of communication systems.

~~2. General description of the invention~~

Variety of the high resolution phase detectors are described in this document using the same terms which are explained below.

First signal clock f_{F1} is a higher frequency signal which is used to measure time periods corresponding to single or multiple cycles of a lower frequency signal which is called second signal frame fr_{S2}.

High resolution phase detectors comprise:

- a counter and a buffer configuration for counting the first signal clock during every frame of a second signal, and for buffering the counted value until it is read by a phase processing unit;
- a high resolution extension of the counter and buffer configuration, which measures a remainder of a frame phase skew which is lesser than one clock cycle;
- a detector timing circuit for synchronizing the clock counting and the buffer reading versus the signal frame related phase capture into a phase capture register;
- a high resolution phase processing method for combining contents of the clock counter and the phase capture register into a high resolution phase measurement.

The high resolution extension can be implemented by using a propagation circuit and a phase capture register, as it is explained below.

The first signal clock or the measured second signal frame is propagated through multiple serially connected gates.

The first signal clock or the second signal frame is captured in the phase capture register by the outputs of the serially connected gates, or the outputs of the serially connected gates are captured in the phase capture register by the first signal clock or by the second signal frame. The content of the phase capture register is used to calculate a phase skew of the second signal frame versus the first signal clock.

The high resolution phase processing method comprises:

- a calculation of an approximate phase error between the first signal and the second signal, by subtracting a number of first signal clock cycles which corresponds to zero phase skew of the second signal frame, from a last number of clock cycles which has been read from the buffer;
- a calculation of a high resolution phase error by adding the high resolution extension to the approximate phase error;
- elimination of phase error accumulations for multiple measurements, by subtracting last high resolution extension from a period of the first signal clock, and by adding the resulting remainder of the clock cycle to an adjacent phase error measurement.

The above ~~design principles and~~ methods allow designing multiple different implementations of HRPD.

Some of these HRPD implementations are defined ~~below~~ in the GENERAL DESCRIPTION OF THE INVENTION and are shown with more details in the ~~section~~ DESCRIPTION OF THE PREFERRED EMBODIMENTS.

BRIEF DESCRIPTION OF THE DRAWINGS

HRPD implementations and preferred embodiments of the invention will now be described with reference to attached drawings in which:

FIG.1 shows Circuits of the HRPD Config.1 based on an open ended delay line captured by frame edge. FIG.2 shows timing analysis of the HRPD Config.1.

FIG.3 shows High Resolution Extension of the HRPD Config.2 based on a ring oscillator captured by frame edge.

FIG.4 shows High Resolution Extension of the HRPD Config.3 based on clock signal captured by frame delay line edges.

FIG.5 shows Detector Timing Circuit of the HRPD Config.3, which solves most critical timing of the HRPD Config.3. FIG.6 shows Timing Analysis of the HRPD Config.3.

FIG.7 shows High Resolution Extension of the HRPD Config.4 based on frame delay line captured by clock signal.

FIG.8 shows Detector Timing Circuit of the HRPD Config.4, while FIG.9 shows resulting Timing Analysis of the HRPD Config.4.

FIG.10 shows High Resolution Extension of the HRPD Config.5 based on frame captured by clock delay line.

FIG.11 shows Detector Timing Circuit of the HRPD Config.5, while FIG.12 shows resulting Timing Analysis of the HRPD Config.5.

FIG.13 shows High Resolution Extension of the HRPD Config.6 based on frame captured by ring oscillator, while FIG.14 shows resulting Timing Analysis of the HRPD Config.6.

GENERAL DESCRIPTION OF THE INVENTION

~~3.~~ 1. HRPD Config.1 based on delay line captured by frame edge

The HRPD Config.1 uses:

- an open ended delay line which is built with multiple serially connected gates, which the first signal clock is continuously propagated through;
- a leading edge of the second signal frame to capture a status of the outputs of the delay line in the phase capture register;
- a calibration method of gates propagation delays, which is based on capturing the whole cycle of the first signal clock as it is propagated along the delay line and dividing the first

signal cycle time by the number of gates which carried the whole cycle propagation.

The calibration method comprises:

- statistical averaging of the calibration result, in order to eliminate most of a granularity error caused by capturing of the integer gates number and to reduce an error caused by power supply ripple.

The calibration method can further comprise a reduction of an error caused by an occurrence of different gate delays at the end versus the front of the delay line:

- by assigning higher weights to the cycle gate number, if captured cycle propagating gates are located at the front of the delay line;
- by using the weighted cycle gate numbers for the statistical averaging of the calibration result.

~~4.~~ 2. HRPD Config.2 based on ring oscillator captured by frame edge.

The HRPD Config.2 uses:

- the signal propagation circuit which is built with multiple serially connected gates forming a ring oscillator which is phase locked to the first signal clock;
- a leading edge of the second signal frame to capture a status of the outputs of the ring oscillator gates in the phase capture register.

Since the number of ring oscillator gates and the first signal clock period are known, calibration of gates propagation delay is not needed for the HRPD Config.2.

~~5.~~ 3. HRPD Config.3 based on clock signal captured by frame delay line edges.

The HRPD Config.3 uses:

- the signal propagation circuit which is built with multiple serially connected gates forming an open ended delay line, which the second signal frame is continuously propagated

through;

- the outputs of the delay line gates to capture a waveform of the first signal clock, in the phase capture register;
- a calibration method of gates propagation delays, which is based on capturing the whole cycle of the first signal clock as it occurs along the inputs of the phase capture register, and dividing the first signal cycle time by the number of the delay line gates which outputs captured the whole clock cycle.

The calibration method comprises:

- statistical averaging of the calibration result, in order to eliminate most of a granularity error caused by having an integer number of the capturing gates, and to reduce an error caused by power supply ripples.

The calibration method can further comprise a reduction of an error caused by an occurrence of different gate delays at the end versus the front of the delay line:

- by assigning higher weights for the cycle capturing gate number, if the cycle capturing gates are located at the front of the delay line;
- by using the weighted cycle gate numbers for the statistical averaging of the calibration result.

~~6.~~ 4. HRPD Config.4 based on frame delay line captured by clock signal.

The HRPD Config.4 uses:

- the signal propagation circuit which is built with multiple serially connected gates forming an open ended delay line, which the second signal frame is continuously propagated through;
- the outputs of the delay line gates are captured by rising edges of the first signal clock in phase capture registers;
- a calibration method of gates propagation delays which is based on capturing the frame delay

line by 2 consecutive first signal rises, and dividing the first signal cycle time by a difference between numbers of gate delays which were captured by the consecutive first signal rises.

The calibration method comprises:

- statistical averaging of the calibration result, in order to eliminate most of a granularity error caused by capturing an integer number of the delay line gates, and to reduce an error caused by power supply ripples.

The calibration method can further comprise a reduction of an error caused by an occurrence of different gate delays at the end versus the front of the delay line:

- by assigning higher weights to the cycle capturing gate number, if the cycle capturing gates are located at the front of the delay line;
- by using the weighted cycle gate numbers for the statistical averaging of the calibration result

~~7.~~ 5. HRPD Config.5 based on frame captured by clock delay line.

The HRPD Config.5 uses:

- the signal propagation circuit which is built with multiple serially connected gates forming an open ended delay line, which the first signal clock is continuously propagated through;
- the outputs of the delay line gates to capture a rise of the second signal frame in the phase capture register;
- a calibration method of gates propagation delays which is based on:
  - capturing a frame rising edge by two consecutive rising edges of the signal clock which occur simultaneously along the delay line;
  - and dividing the first signal cycle time by a number of delay line gates which existed between said clock edges when they captured simultaneously the frame rising edge in the capture register;

- a capture synchronization method which prevents the next propagated clock edges from overwriting said captures of the frame rise by said two consecutive clock edges.

The calibration method comprises:

- statistical averaging of the calibration result, in order to eliminate most of a granularity error caused by having an integer number of the capturing gates, and to reduce an error caused by power supply ripples.

The calibration method can further comprise a reduction of an error caused by an occurrence of different gate delays at the end versus the front of the delay line:

- by assigning higher weights to the cycle capturing gate number, if the cycle capturing gates are located at the front of the delay line.
- by using the weighted cycle gate numbers for the statistical averaging of the calibration result

~~8.~~ 6. HRPD Config.6 based on frame captured by ring oscillator.

The HRPD Config.6 uses:

- outputs of the signal propagation circuit, which is built with multiple serially connected gates forming a ring oscillator which is phase locked to the first signal clock;
- the outputs of the ring oscillator gates to capture a rise of the second signal frame in the phase capture register;
- a capture synchronization method which prevents next propagated clock edges from overwriting said capture of the rise of the second signal frame.

Since the number of ring oscillator gates and the first signal clock period are known, calibration of gates propagation delay is not needed for the HRPD Config.6.

Claim Amendments

Please replace all the original claims with the claims listed below.

1. (currently amended) A digital phase detector for measuring a phase skew between a first signal frame consisting of a nominal number of first signal clocks and a second signal frame, wherein ~~the digital phase detector comprises~~:
a frame measurement configuration is used for counting the first signal clock during every frame of a second signal, and for buffering the counted value until it is read by a phase processing unit~~.~~;
a subtracting circuit is used for subtracting the nominal number of first signal clocks from the counted number of the first signal clocks, in order to calculate an approximate phase skew between the first signal frame and the second signal frame.

2. (canceled)

3. (currently amended) A digital phase detector as claimed in claim 1, wherein:
~~a number~~ said subtracting circuit presets a counter of the first signal clock~~s which equals~~ to zero minus the nominal number of first signal clocks~~, is preset in a counter of the first signal clock~~ before the first clock counting for every second signal frame.

4. (original) A digital phase detector as claimed in claim 1, further comprising:
a phase capture register for capturing a state of outputs of serially connected gates which the first signal clock is propagated through, at the leading edge of the second signal frame.

5. (original) A digital phase detector as claimed in claim 1, further comprising:
a phase capture register for capturing a rise of the second signal frame by multiple outputs of serially connected gates which the first signal clock is propagated through.

6. (original) A digital phase detector as claimed in claim 1, further comprising:
a phase capture register for capturing a state of outputs of serially connected gates which the second signal frame is propagated through, by the leading edge of the first signal clock.

7. (original) A digital phase detector as claimed in claim 1, further comprising:
a phase capture register for capturing a rise of the first signal clock, by multiple outputs of serially connected gates which the second signal frame is propagated through.

8. (original) A digital phase detector as claimed in claim 4 or in claim 5 or in claim 6 or in claim 7, wherein the digital phase detector comprises:
an open ended line of serially connected components which are used as the serially connected gates.

9. (original) A digital phase detector as claimed in claim 4 or in claim 5 or in claim 6 or in claim 7, wherein the digital phase detector comprises:
a ring oscillator which gates are used as the serially connected gates.

10. (original) A digital phase detector as claimed in claim 4 or in claim 5 or in claim 6 or in claim 7, wherein the digital phase detector comprises:
a delay locked loop which gates are used as the serially connected gates.

11. (original) A digital phase detector as claimed in claim 1, the digital phase detector comprising:
a first phase counter buffer for counting first signal clocks during every odd cycle of the second signal frame, and for buffering the counted clocks number during every following even cycle of the second signal frame;
a second phase counter buffer for counting first signal clocks during every even cycle of the second signal frame, and for buffering the counted clocks number during every following odd cycle of the second frame.

12. (original) A digital phase detector as claimed in claim 11, wherein the digital phase detector comprises:
a detector timing circuit for controlling the counting and the buffering functions of the first and the second phase counter buffers.

13. (original) A digital phase detector as claimed in claim 11, wherein said detector timing circuit further comprises:
detection of a beginning of a cycle of the second signal frame;
switching the counter buffers into the counting and buffering operations;
requesting the phase processing unit to read the buffered count numbers;

14. (original) A digital phase detector as claimed in claim 11, wherein:
the first counter buffer is reset after its content is read by a phase processing unit;
the second counter buffer is reset after its content is read by the phase processing unit.

15. (canceled)

16. (original) A digital phase detector as claimed in claim 11, wherein:
the first counter buffer is preset to zero minus the nominal number of first signal clocks, after its content is read by the phase processing unit;
the second counter buffer is preset to zero minus the nominal number of first signal clocks, after its content is read by the phase processing unit.

17. (currently amended) A digital phase detector as claimed in claim 1, wherein:
said first clock counting is enabled by opening a logical gate which controls an application of the first clock to a clocking input of a first clock counter ~~counter's clocking input~~;
said first clock counting is disabled by closing a logical gate which controls an application of the first clock to the clocking input of the first clock counter ~~counter's clocking input~~.

18. (original) A digital phase detector as claimed in claim 4 or in claim 5 or in claim 6 or in claim 7, wherein:
a content of the phase capture register is used to calculate a phase skew difference between the last rise of the first signal clock and the beginning of a new second signal frame;
a content of the phase capture register is used to calculate a remaining phase skew between the beginning of a new second signal frame and the first rise of the first signal clock.

19. (original) A digital phase detector as claimed in claim 18, wherein:
the phase skew difference is added to the present measurement of a phase skew between the first signal and the second signal, wherein the present measurement applies to the present frame period of the second signal;
the remaining phase skew is added to the next measurement of a phase skew between the first signal and the second signal, wherein the next measurement applies to the next frame period of the second signal.

20. (original) A digital phase detector as claimed in claim 18, wherein:
the remaining phase skew is calculated as equal to the first signal clock period minus the phase skew difference.

21. (original) A digital phase detector as claimed in claim 18, wherein:
a content of the phase capture register is used to upgrade the counted number of first signal clocks to an actual number of first signal clocks which really occurred during the second signal frame.

22. (original) A digital phase detector as claimed in claim 8, wherein the digital phase detector comprises a calibration method of gates propagation delays, wherein:
a number of the serially connected gates which represents a number of half cycle times of the first signal clock, is captured in the phase capture register;

the number of half cycle times of the first signal clock, is divided by the captured number.

23. (original) A digital phase detector as claimed in claim 22, wherein the calibration method comprises:
a statistical averaging of a result of the calibration, in order to eliminate most of a granularity error caused by capturing of an integer and to reduce an error caused by a power supply ripple.

24. (original) A digital phase detector as claimed in claim 23, wherein the calibration method further comprises:
assigning higher weights for the captured number of gates, if the captured number is provided by serially connected gates which are located at the front of the delay line;
using the weighted cycle gate numbers for the statistical averaging of the calibration result.

25. (original) A digital phase detector as claimed in claim 4 or in claim 5 or in claim 6 or in claim 7, wherein the digital phase detector comprises:
a first phase counter buffer for counting first signal clocks during every odd cycle of the second signal frame, and for buffering the counted clocks number during every following even cycle of the second signal frame;
a second phase counter buffer for counting first signal clocks during every even cycle of the second signal frame, and for buffering the counted clocks number during every following odd cycle of the second frame.
a detector timing circuit for switching the counting and the buffering functions of the first and the second phase counter buffer.

26. (original) A digital phase detector as claimed in claim 25, wherein:
the switching performed by the detector timing circuits is driven by the first signal clock and is conditioned by a content of the phase capture register.

27. (original) A digital phase detector as claimed in claim 25, wherein:

the phase capture register and some of the flip-flops of the detector timing control, are reset outside of a close time range which surrounds a rising edge of every second signal frame.

28. (original) A digital phase detector as claimed in claim 25, wherein:
if a rising edge of the second signal frame encounters a high level of the first signal clock, the second falling edge of the first signal clock will reverse the counting and the buffering functions of the first and the second phase counter buffer;
if a rising edge of the second signal frame encounters a low level of the first signal clock, the first falling edge of the first signal clock will reverse the counting and the buffering functions of the first and the second phase counter buffer.

29. (original) A digital phase detector as claimed in claim 25, wherein the detector timing circuit comprises a function switching flip-flop, wherein:
the function switching flip-flop switched to 1, inhibits counting in the first counter buffer and enables counting in the second counter buffer;
the function switching flip-flop switched to 0, inhibits counting in the second counter buffer and enables counting in the first counter buffer.

30. (original) A digital phase detector as claimed in claim 11, wherein the digital phase detector further comprises:
a detector timing circuit for switching the counting and the buffering functions of the first and the second phase counter buffer.

31. (original) A digital phase detector as claimed in claim 30, wherein the detector timing circuit further comprises a function switching flip-flop, wherein:
the function switching flip-flop switched to 1, inhibits counting in the first counter buffer and enables counting in the second counter buffer;
the function switching flip-flop switched to 0, inhibits counting in the second counter buffer and enables counting in the first counter buffer.

32. (original) A digital phase detector as claimed in claim 31, wherein the digital phase detector further comprises:
a phase capture register for capturing a state of outputs of serially connected gates which the first signal clock is propagated through, at the leading edge of the second signal frame;
an open ended line of serially connected components which are used as the serially connected gates.

33. (original) A digital phase detector as claimed in claim 31, wherein the digital phase detector further comprises:
a phase capture register for capturing a state of outputs of serially connected gates which the first signal clock is propagated through, at the leading edge of the second signal frame;
a ring oscillator which gates are used as the serially connected gates.

34. (original) A digital phase detector as claimed in claim 31, wherein the digital phase detector further comprises:
a phase capture register for capturing a rise of the first signal clock, by multiple outputs of serially connected gates which the second signal frame is propagated through;
an open ended line of serially connected components which are used as the serially connected gates.

35. (original) A digital phase detector as claimed in claim 31, wherein the digital phase detector further comprises:
a phase capture register for capturing a state of outputs of serially connected gates which the second signal frame is propagated through, by the leading edge of the first signal clock.
an open ended line of serially connected components which are used as the serially connected gates.

36. (original) A digital phase detector as claimed in claim 31, wherein the digital phase detector

further comprises:

a phase capture register for capturing a rise of the second signal frame by multiple outputs of serially connected gates which the first signal clock is propagated through;

an open ended line of serially connected components which are used as the serially connected gates.

37. (original) A digital phase detector as claimed in claim 31, wherein the digital phase detector further comprises:

a phase capture register for capturing a rise of the second signal frame by multiple outputs of serially connected gates which the first signal clock is propagated through;

a ring oscillator which gates are used as the serially connected gates.

38. (currently amended) A digital phase detector as claimed in claim 32 or in claim 33 or in claim 34 or in claim 35 or in claim 36 or in claim 37, wherein:

~~an approximate frame skew is calculated as equal to the counted number of clock cycles minus the nominal number of first signal clocks;~~

a content of the phase capture register is used to calculate a phase skew difference between the last rise of the first signal clock and the beginning of a new second signal frame;

a content of the phase capture register is used to calculate a remaining phase skew between the beginning of a new second signal frame and the first rise of the first signal clock;

a high resolution extension is calculated by adding the remaining phase skew of the previous measurement to the phase skew difference of the present measurement;

a high resolution frame skew is calculated by adding the approximate frame skew to the high resolution extension.

39. (original) A digital phase detector as claimed in claim 32 or in claim33, wherein:

bit 0 of the phase capture register is set to 1, if a rising edge of the second signal frame encounters a high level of the first signal clock;

bit 1 of the phase capture register is set to 1, if a rising edge of the second signal frame

encounters a low level of the first signal clock;

if the bit 0 is set to 1, it enables a second falling edge of the first signal clock to reverse the function switching flip-flop;

if the bit 1 is set to 1, it enables a first falling edge of the first signal clock to reverse the function switching flip-flop.

40. (original) A digital phase detector as claimed in claim 34, wherein:

bit 0 of the phase capture register is set to 1, if a rising edge of the second signal frame encounters a high level of the first signal clock;

bit -1 of the phase capture register is set to 1, if a rising edge of the second signal frame encounters a low level of the first signal clock;

if the bit 0 is set to 1, it enables a second falling edge of the first signal clock to reverse the function switching flip-flop;

if the bit -1 is set to 1, it enables a first falling edge of the first signal clock to reverse the function switching flip-flop.

41. (original) A digital phase detector as claimed in claim 35 or in claim36 or in claim 37, wherein:

bit -1 of the phase capture register is set to 1, if a falling edge of the first signal clock encounters a high level of the second signal frame before a rising edge of the first signal clock does;

bit 0 of the phase capture register is set to 1, if a rising edge of the first signal clock encounters a high level of the second signal frame before a falling edge of the first signal clock does;

if the bit -1 is set to 1, it enables a second falling edge of the first signal clock to reverse the function switching flip-flop;

if the bit 0 is set to 1, it enables a first falling edge of the first signal clock to reverse the function switching flip-flop.